Title: NOVEL STRUCTURE AND METHOD FOR INTERRUPT DETECTION AND PROCESSING
Assignee: Intel Corporation

REMARKS

This paper responds to the Office Action mailed on <u>January 24</u>, 2006.

Claims 1, 3, 4, 6, 9, 13-17, 19-22, and 24-27. Claims 1-27 remain pending in this application.

Claim Objections

Claim 1 was objected to for reciting the subject matter "the interrupt information" in lines 5-6. However, it has not been specifically clarified in claim 1. For clarity, claim 1 is amended to recite "an interrupt information". Applicant requests reconsideration and withdrawal of the objection.

§102 Rejection of the Claims

Claims 13-16, 18-22, and 24-27 were rejected under 35 USC § 102(b) as being anticipated by Athenes et al. (U.S. 6.192.441 B1, hereinafter Athenes).

Applicant respectfully traverses for at least the reasons presented below.

Claim 13 is amended and recites, among other things, "a configuration circuit configured to store configuration address indicating a location in the memory device to store the interrupt information, wherein the configuration circuit is further configured to store configuration data indicating a number of devices the integrated circuit is configured to handle".

Applicant believes that claim 13 is not anticipated by Athenes because Applicant is unable to find in Athenes everything recited in claim 13. For example, Applicant is unable to find in Athenes "a configuration circuit configured to store configuration address indicating a location in the memory device to store the interrupt information, wherein the configuration circuit is further configured to store configuration data indicating a number of devices the integrated circuit is configured to handle". Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 13.

Dependent claims 14-16 and 18-20 depend from claim 13 and recite the things of claim

13. Thus, Applicant believes that claims 14-16 and 18-20 are not anticipated by Athenes for at least the reasons presented above regarding claim 13, plus the additional things recited in claims

Filing Date: March 30, 2004 Title: NOVEL STRUCTURE AND METHOD FOR INTERRUPT DETECTION AND PROCESSING Assignee: Intel Corporation

14-16 and 18-20. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claims 14-16 and 18-20.

Claim 21 is amended and recites, among other things, "wherein the chipset includes an interrupt controller having a configuration circuit, wherein the configuration circuit is configured to store configuration address indicating a location in the memory device to store the interrupt information, and wherein the configuration circuit is further configured to store configuration data indicating a number of devices the interrupt controller is configured to handle".

Applicant believes that claim 21 is not anticipated by Athenes because Applicant is unable to find in Athenes everything recited in claim 21. For example, Applicant is unable to find in Athenes "wherein the chipset includes an interrupt controller having a configuration circuit, wherein the configuration circuit is configured to store configuration address indicating a location in the memory device to store the interrupt information, and wherein the configuration circuit is further configured to store configuration data indicating a number of devices the interrupt controller is configured to handle". Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 21.

Dependent claims 22 and 24-27 depend from claim 21 and recite the things of claim 21. Thus, Applicant believes that claims 22 and 24-27 are not anticipated by Athenes for at least the reasons presented above regarding claim 21, plus the additional things recited in claims 22 and 24-27. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claims 22 and 24-27.

\$103 Rejection of the Claims

Claims 1-3 and 5 were rejected under 35 USC § 103(a) as being unpatentable over Jeddeloh (U.S. 5,935,233) in view of Athenes.

Applicant respectfully traverses for at least the reasons presented below.

Claim 1 is amended and recites, among other things, "a configuration circuit configured to store configuration address indicating a location in the memory device to store the interrupt information, wherein the configuration circuit is further configured to store configuration data indicating a number of devices the integrated circuit is configured to handle".

Filing Date: March 30, 2004
Title: NOVEL STRUCTURE AND METHOD FOR INTERRUPT DETECTION AND PROCESSING
Assignee: Intel Corporation

Applicant believes that claim 1 is patentable over Jeddeloh and Athenes because

Applicant cannot find a motivation to combine Jeddeloh and Athenes as proposed by the Office

Action

Applicant also believes that claim 1 is patentable over Jeddeloh and Athenes because
Applicant is unable to find in Jeddeloh and Athenes everything recited in claim 1. For example,
Applicant is unable to find in Jeddeloh and Athenes, whether considered individually or in
combination, "a configuration circuit configured to store configuration address indicating a
location in the memory device to store the interrupt information, wherein the configuration
circuit is further configured to store configuration data indicating a number of devices the
integrated circuit is configured to handle". Accordingly, Applicant requests reconsideration and
withdrawal of the rejection, and allowance of claim 1.

Dependent claims 2, 3, and 5 depend from claim 1 and recite the things of claim 1. Thus, Applicant believes that claims 2, 3, and 5 are also patentable over Jeddeloh and Athenes, whether considered individually or in combination, for at least the reasons presented above regarding claim 1, plus the additional things recited in claims 2, 3, and 5. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claims 2, 3, and 5.

Claim 4 was rejected under 35 USC § 103(a) as being unpatentable over Jeddeloh in view of Athenes as applied to claims 1-3 and 5 above, and further in view of Tseng et al. (U.S. 6,816,918 B2).

Applicant respectfully traverses for at least the reasons presented below.

Dependent claim 4 depends from claim 1 and recites the things of claim 1. Applicant believes that claim 4 is patentable over Jeddeloh, Athenes, and Tseng, whether considered individually or in combination, for at least the reasons presented above regarding claim 1, plus the additional things recited in claim 4. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claim 4.

Claims 6-11 were rejected under 35 USC § 103(a) as being unpatentable Watson et al. (U.S. 6,466,226 B1, hereinafter Watson) in view of Athenes (U.S. 6,192,441 B1).

Applicant respectfully traverses for at least the reasons presented below.

Claim 6 is amended and recites, among other things, "the chipset includes an interrupt controller having a configuration circuit, wherein the configuration circuit is configured to store AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111 Serial Number: 10/813,602 Filing Date: March 30, 2004

Title: NOVEL STRUCTURE AND METHOD FOR INTERRUPT DETECTION AND PROCESSING
Assignee: Intel Corporation

configuration address indicating a location in the memory device to store the interrupt information, and wherein the configuration circuit is further configured to store configuration data indicating a number of devices the interrupt controller is configured to handle".

Applicant believes that claim 6 is patentable over Watson and Athenes because Applicant cannot find a motivation to combine Watson and Athenes as proposed by the Office Action.

Applicant also believes that claim 6 is patentable over Watson and Athenes because
Applicant is unable to find in Watson and Athenes everything recited in claim 6. For example,
Applicant is unable to find in Watson and Athenes, whether considered individually or in
combination, "the chipset includes an interrupt controller having a configuration circuit, wherein
the configuration circuit is configured to store configuration address indicating a location in the
memory device to store the interrupt information, and wherein the configuration circuit is further
configured to store configuration data indicating a number of devices the interrupt controller is
configured to handle". Accordingly, Applicant requests reconsideration and withdrawal of the
rejection, and allowance of claim 6.

Dependent claims 7-11 depend from claim 6 and recite the things of claim 6. Thus, Applicant believes that claims 7-11 are also patentable over Watson and Athenes, whether considered individually or in combination, for at least the reasons presented above regarding claim 6, plus the additional things recited in claims 7-11. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claims 7-11.

Claim 12 was rejected under 35 USC § 103(a) as being unpatentable over Watson in view of Athenes as applied to claim 6-11 above, and further in view of what was well known in the art, as exemplified by Callway et al. (U.S. 6,279,067 B1, hereinafter Callway).

Applicant respectfully traverses for at least the reasons presented below.

Applicant believes that claim 12 is patentable over Watson, Athenes, and Callway because Applicant cannot find a motivation to combine Watson, Athenes, and Callway as proposed by the Office Action. Moreover, since claim 12 depends from claim 6, Applicant also believes that claim 12 is patentable over Watson, Athenes, and Callway, whether considered individually or in combination, for at least the reasons presented above regarding claim 6, plus the additional things recited in claim 12.

Filing Date: March 30, 2004

Fring Date: March 30, 2004
Title: NOVEL STRUCTURE AND METHOD FOR INTERRUPT DETECTION AND PROCESSING
Assignee: Intel Corporation

Further, the Office Action refers to a system taught by Callway for an example of a second processor that performs the polling. However, Callway appears to teach a different system. The Official Action takes Official Notice to reject claim 12. Applicant respectfully traverses the taking of Official Notice and, pursuant to M.P.E.P. § 2144.03, Applicant requests documents or an affidavit to support the rejection of claim 12. Notwithstanding the above reasons regarding the patentability of claim 12, in the absence of documents or an affidavit to support the rejection of claim 12, Applicant requests reconsidered, withdrawal of the rejection, and allowance of claim 12.

Claims 17 and 23 were rejected under 35 USC § 103(a) as being unpatentable over Athenes as applied to claim 13-16, 18-22, and 24-27 above, and further in view of Callway.

Applicant respectfully traverses for at least the reasons presented below.

Applicant believes that claim 17 is patentable over Athenes and Callway because

Applicant cannot find a motivation to combine Athenes and Callway as proposed by the Office

Action. Moreover, since claim 17 depends from claim 13, Applicant also believes that claim 17

is patentable over Athenes and Callway, whether considered individually or in combination, for

at least the reasons presented above regarding claim 13, plus the additional things recited in

claim 17.

Applicant believes that claim 23 is patentable over Athenes and Callway because

Applicant cannot find a motivation to combine Athenes and Callway as proposed by the Office

Action. Moreover, since claim 23 depends from claim 21, Applicant also believes that claim 23

is patentable over Athenes and Callway, whether considered individually or in combination, for

at least the reasons presented above regarding claim 21, plus the additional things recited in

claim 23.

Assignee: Intel Corporation

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((612) 373-6969) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

PETER C. BRINK ET AL.

By their Representatives, SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. Attomeys for Intel Corporation P.O. Box 2938 Minneapolis, Minnesota 55402 (612) 373-6969

Date 24 April 2006

Viet V. Tong Reg. No. 45.416

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner for Patents, P.O. Box 1450,

Alexandria, VA 22313-1450, on this 24th day of April, 2006.

Nama

Signature